CLAIMS

What is claimed is:

1. A memory device comprising:

a substrate having a first semiconductor bitline and a second semiconductor bitline formed therein and a body region interposed between the first and second bitlines;

a bottom dielectric layer disposed over the body region;

a non-conductive charge trapping layer disposed over the bottom dielectric layer, said non-conductive charge trapping layer being operatively configured to have at least two independent charge storing regions;

a top dielectric stack disposed over the non-conductive charge trapping layer, said top dielectric stack including at least three dielectric layers; and

a wordline disposed over the top dielectric stack and electrically defining a channel within the body region.

2. The memory device according to claim 1, wherein the top dielectric stack has a thickness of about 50 angstroms to about 90 angstroms.

3. The memory device according to claim 1, wherein the top dielectric stack includes:

a first oxide layer disposed over the charge trapping layer;

at least one of (i) a nitride layer and (ii) an aluminum oxide layer disposed over the first oxide layer; and

a second oxide layer disposed over the at least one of (i) a nitride layer and (ii) aluminum oxide layer.

4. The memory device according to claim 3, wherein the first and second oxide layers are silicon dioxide.

5. The memory device according to claim 3, wherein:

the first oxide layer has a thickness of about 10 angstroms to about 30 angstroms;

the at least one of (i) a nitride layer and (ii) an aluminum oxide layer has a thickness of about 30 angstroms to about 50 angstroms; and

the second oxide layer has a thickness of about 10 angstroms to about 30 angstroms.

6. The memory device according to claim 3, wherein the top dielectric stack has a physical thickness greater than a thickness of the bottom dielectric layer and an electrical thickness that is less than an electrical thickness of the bottom dielectric layer.

7. The memory device according to claim 6, wherein:

the charge trapping layer has a conductivity such that at least a first charge can be stored in a first charge trapping cell adjacent the second bitline and at least a second charge can be stored in a second charge trapping cell adjacent the first bitline; and

the top dielectric stack is effective to increase the probability that charge will be stored in at least one of the first and second charge trapping cells upon application of a voltage potential of less than about +8 Volts to the wordline.

8. A method of programming the memory device according to claim 6, said method including:

applying a program voltage of less than about +8 Volts to the wordline;

applying a voltage potential of about +3 Volts to about +5 Volts to the first bitline; and

one of (i) connecting the second bitline to a zero potential, and (ii) floating the second bitline.

9. The memory device according to claim 6, said memory device being operative to be erased by a hot hole injection erase operation.

10. A memory device comprising:

a semiconductor substrate;

a source and a drain formed from buried bitlines disposed within the semiconductor substrate, said source and drain defining a body region therebetween;

a charge trapping dielectric stack having at least 5 dielectric layers formed over the body region and including a non-conductive charge trapping layer; and

a gate electrode formed from a wordline disposed over the charge trapping dielectric stack, said gate electrode electrically defining a channel within the body region.

11. The memory device according to claim 10, wherein the charge trapping dielectric stack includes:

a first dielectric layer disposed over the body region;

a charge trapping dielectric layer disposed over the first dielectric layer;

a second dielectric layer disposed over the charge trapping dielectric layer;

a third dielectric layer disposed over the second dielectric layer; and

a fourth dielectric layer disposed over the third dielectric layer.

12. The memory device according to claim 11, wherein the charge trapping dielectric layer and the third dielectric layer are comprised of a nitride material; and

the first, second and fourth dielectric layers are comprised of an oxide material.

13. The memory device according to claim 10, wherein the charge trapping dielectric stack includes:

a bottom dielectric layer formed over the body region;

a charge trapping dielectric layer formed over the bottom dielectric layer; and

a top dielectric stack formed over the charge trapping dielectric layer.

14. The memory device according to claim 13, wherein the top dielectric stack includes:

a first oxide layer formed over the charge trapping dielectric layer;

at least one of (i) a nitride layer and (ii) an aluminum oxide layer formed over the first oxide layer; and

a second oxide layer formed over the nitride layer.

15. The memory device according to claim 14, wherein the top dielectric stack has a thickness of about 50 angstroms to about 90 angstroms.

16. The memory device according to claim 14, wherein the top dielectric stack has an electrical thickness less than an electrical thickness of the bottom dielectric layer.

17. The memory device according to claim 13, wherein:

the charge trapping dielectric layer has a conductivity such that at least a first charge can be stored in a first charge trapping cell adjacent the drain and at least a second charge can be stored in a second charge trapping cell adjacent the source; and

the top dielectric stack is effective to increase the probability that charge will be stored in at least one of the first and second charge trapping cells upon application of a voltage potential of less than about +8 Volts to the gate electrode.

18. A method of programming the memory device according to claim 13, said method including:

applying a program voltage of less than about +8 Volts to the gate electrode;

applying a voltage potential of about +3 Volts to about +5 Volts to the drain; and

one of (i) connecting the source to a zero potential, and (ii) floating the source.

19. A method of erasing the memory device according to claim 13, said method including:

applying an erase voltage of about -12 Volts to about -15 Volts to the gate electrode; and

connecting the substrate, the source and the drain to a zero potential.

20. A method of programming a non-volatile memory device having a pair of buried bitlines disposed within a semiconductor substrate, said buried bitlines defining a body region therebetween, a bottom dielectric layer formed over the body region, a charge storing layer formed over the bottom dielectric layer, said charge storing layer having a conductivity such that at least a first charge can be stored in a first charge storing cell adjacent a first buried bitline and at least a second charge can be stored in a second charge storing cell adjacent a second buried bitline, a top dielectric stack including at least three dielectric layers formed over the charge storing layer, and a wordline formed over the top dielectric layer, said method comprising:

applying a program voltage of about +6 Volts to about +7.5 Volts to the wordline;

applying a voltage potential of about +3 Volts to about +5 Volts to the first bitline; and

connecting the second bitline to a zero potential.